Product Specification

MODEL NO.:JFC2KLTEDP8801T

Product version: V1.0

Customer: Common Model

APPROVED BY SIGNATURE

Note

1. Be aware of product version.
2. Please contact with JFC when you need any parameters unavailable in this manual

Approved By	Checked By	Prepared By
SIM ZHANG	CHEN SHI	FU YAN QIANG

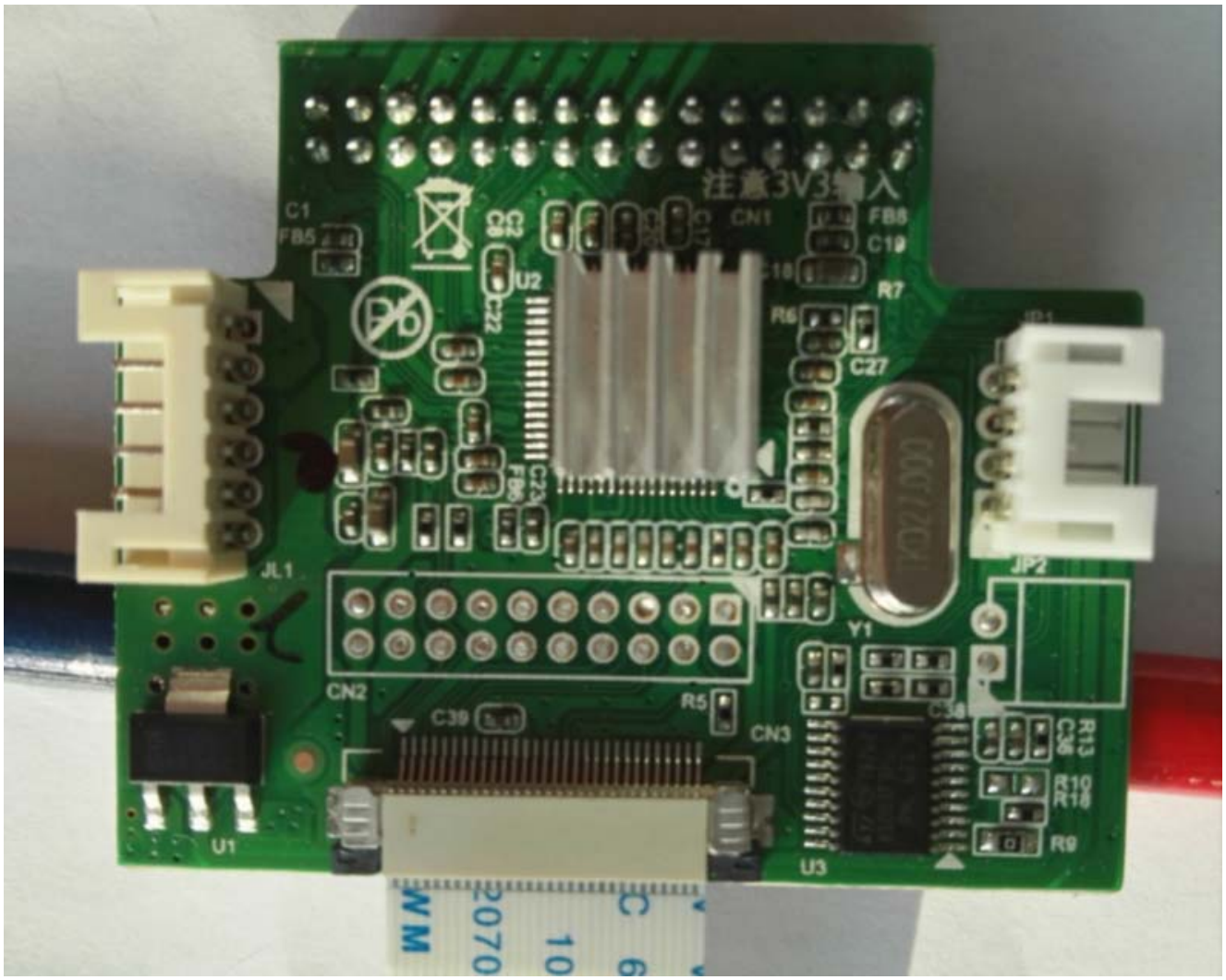
1. GENERAL DESCRIPTION

JFC2KLTEDP8801T Conversion board is mainly used for video / image transmission in the receiving part, the realization of the function of is the high speed serial LVDS signal decoding for data parallel DP/EDP, data decoding function. The board may 8 to serial LVDS differential signal is converted to a DisplayPort output data.

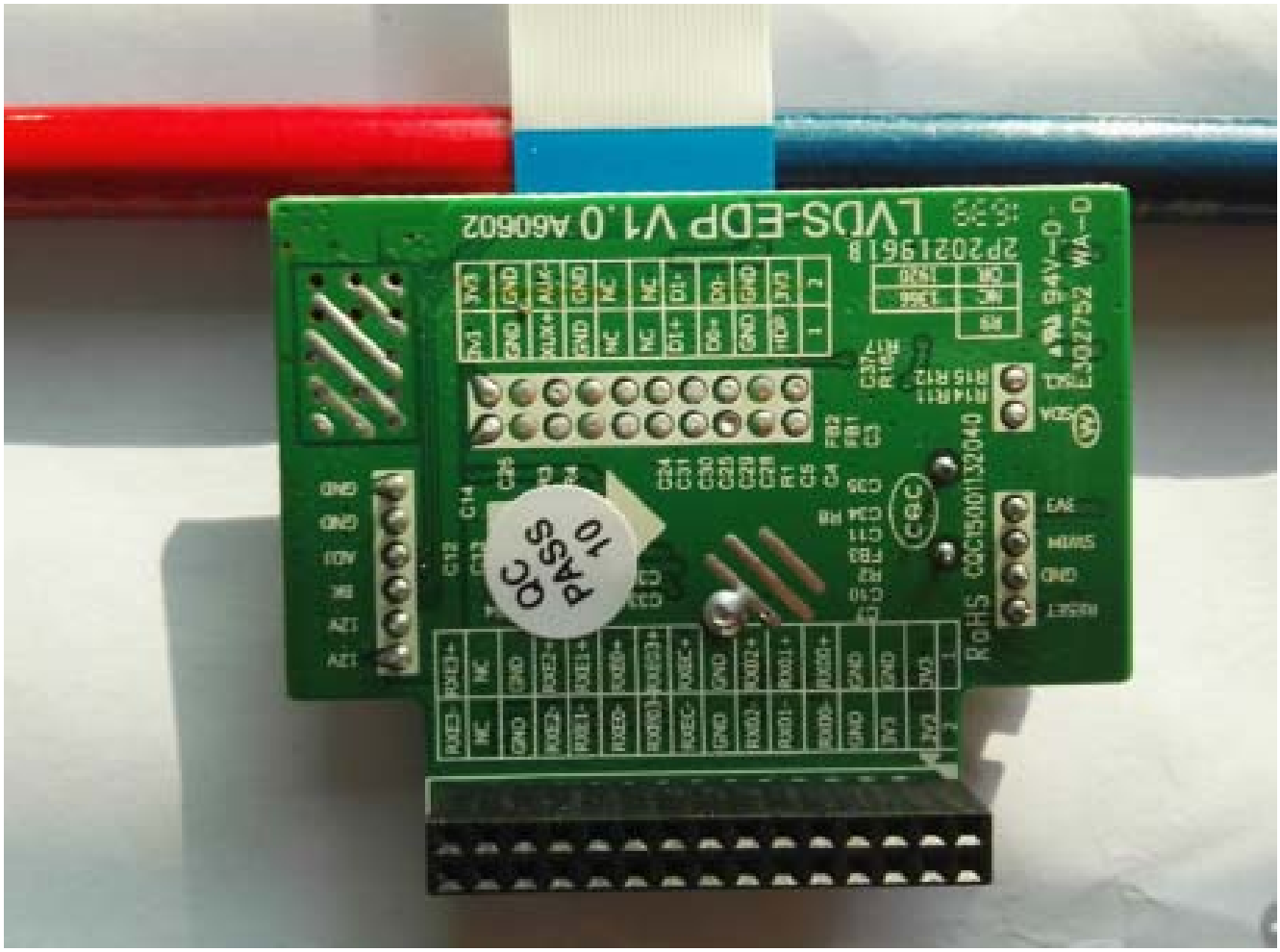
JFC2KLTEDP8801T can support resolution up to 1080P and UXGA and 10-bit deep colors.

2. FUNCTION LAYOUT

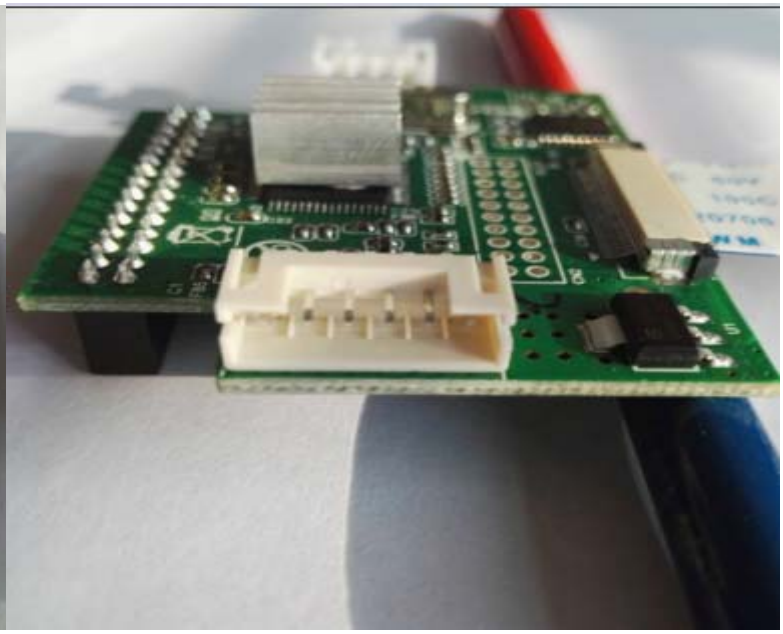
All of pictures below are only for reference. Please take the actual objects as a standard.



Front View Of JFC2KLTEDP8801T



Side Elevation of JFC2KLTEDP8801T



3. FEATURES

Below you will find the detailed feature.

Working Temp.	-40℃～85℃
Power	3.0V~3.6V
Data ratio	4：28
Input	EIA/TIA-644 standard 8 bit LVDS and 1 line LVDS Clock
Output	DP and EDP
Frequency	10MHz～90MHz
Data rate:	2520Mbps
Video	support: VGA，SVGA，SXGA（dual pixel）; UXGA（dual pixel）,up 1080p

4. INTERFACE DEFINITION

CN1(2*15PIN/2.0) LVDS PANEL INTERFACE（LVDS INFOR）

NO.PIN	SYMBOL	DESCRIPTION
1	3V3	Power for panel
2	3V3	
3	GND	Ground
4	3V3	Power for panel
5	GND	Ground
6	GND	Ground
7	RXO0+	LVDS ODD 0+ Signal
8	RXO0-	LVDS ODD 0- Signal
9	RXO1+	LVDS ODD 1+ Signal
10	RXO1-	LVDS ODD 1- Signal
11	RXO2+	LVDS ODD 2+ Signal
12	RXO2-	LVDS ODD 2- Signal
13	GND	Ground
14	GND	

15	RXEC+	LVDS EVEN Clock+ Signal
16	RXEC-	LVDS EVEN Clock- Signal
17	RXO3+	LVDS ODD 3+ Signal
18	RXO3-	LVDS ODD 3- Signal
19	RXE0+	LVDS EVEN 0+ Signal
20	RXE0-	LVDS EVEN 0- Signal
21	RXE1+	LVDS EVEN 1+ Signal
22	RXE1-	LVDS EVEN 1- Signal
23	RXE2+	LVDS EVEN 2+ Signal
24	RXE2-	LVDS EVEN 2- Signal
15	GND	Ground
16	GND	
27	NC	
28	NC	
29	RXE3+	LVDS EVEN 3+ Signal
30	RXE3-	LVDS EVEN 3- Signal

CN2 (2*10PIN/2.0) DP OUTPUT INTERFACE（DP OUTPUT）

NO.PIN	SYMBOL	DESCRIPTION
1	HDP	Hot Plug Detect Signal
2	3V3	3V3 power output
3	GND	Ground
4	GND	Ground
5	D0+	True Signal for Main Link 0
6	D0-	Component Signal for Main Link 0
7	D1+	True Signal for Main Link 1
8	D1-	Component Signal for Main Link 1
9	D2+	True Signal for Main Link 2
10	D2-	Component Signal for Main Link 2

11	D3+	True Signal for Main Link 3
12	D3-	Component Signal for Main Link 3
13	GND	Ground
14	GND	Ground
15	AUX-	Component Signal for Auxiliary Channel
16	AUX+	True Signal for Auxiliary Channel
17	GND	Ground
18	GND	Ground
19	VCC	LCD power output
20	VCC	LCD power output

CN3 (30PIN/1.25) DP OUTPUT INTERFACE（DP OUTPUT FFC）

NO.PIN	SYMBOL	DESCRIPTION
1		NC
2		GND
3		D1-
4		D1+
5		GND
6		D0-
7		D0+
8		GND
9		AUX+
10		AUX-
11		GND
12		3V3
13		3V3
14		NC
15		GND
16		GND
17		HPD
18		GND
19		GND
20		GND
21		GND
22		BK
23		ADJ
24		NC

25		NC
26		+12V
27		+12V
28		+12V
29		+12V
30		GND

JL1(6PIN/2.0)Backlight OUTPUT INTERFACE

NO.PIN	SYMBOL	DESCRIPTION
1	12V	+12V Backlight Power IN
2	12V	+12V Backlight Power IN
3	BK	Enable Pin
4	ADJ	ADJ
5	GND	Ground
6	GND	Ground

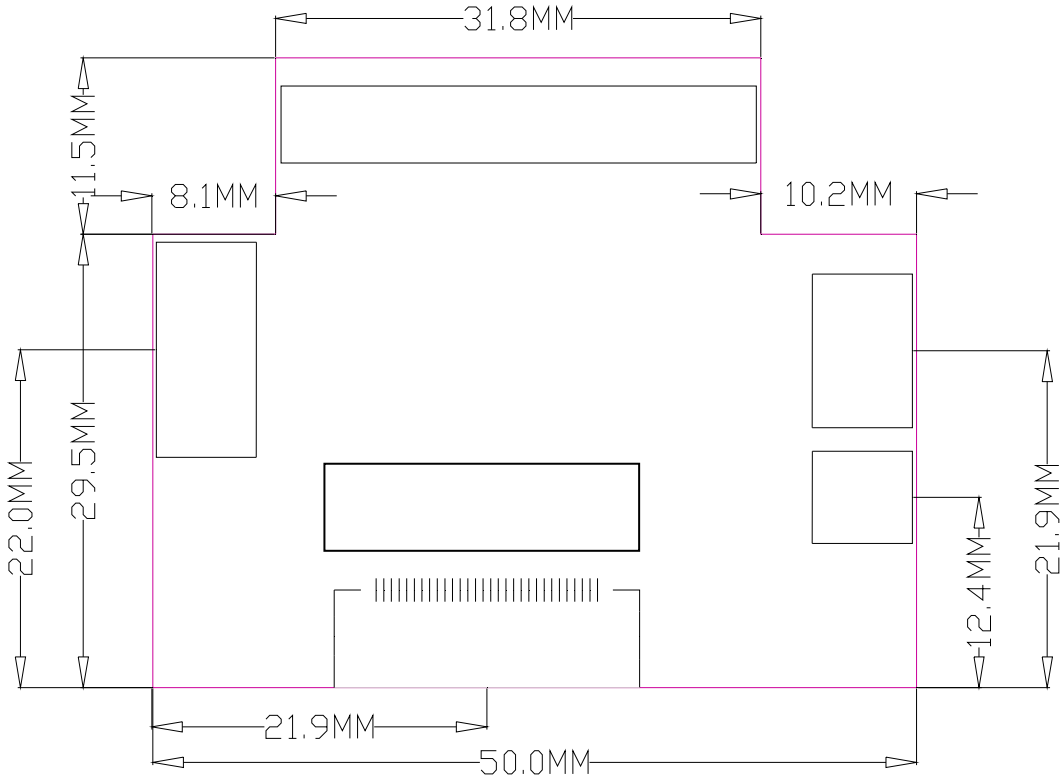
JP1 (4PIN/2.0) DOWNLOAD INTERFACE

NO.PIN	SYMBOL	DESCRIPTION
1	3V3	Power for panel
2	SWIM	
3	GND	
4	RESET	Reset MCU PIN

JP2(2PIN/2.0)I2C INTERFACE (I2C)

NO.PIN	SYMBOL	DESCRIPTION
1	SCL	
2	SDA	

5. CONTROLLER DIMENSIONS（UNIT：mm）



6. ENVIRONMENTAL REQUIREMENT & NOTICE

Do not pressed and distorted.

① Keep away from static and water.

② Relative humidity : 10% ~ 90%.

③ Storage humidity : 5% ~ 95%.

④ Storage temperature: -10~ +60℃.

⑤ Operation temperature: 0~ +40℃.

⑥ Cooling Method: Ventilation cooling.

⑦ The production shall not be exposed to dripping or splashing and that no objects filled with liquids, such as vases, shall be placed on it.

⑧ Please use it under the condition of good aeration.